REMARKS

The present application was filed on October 12, 2001, with claims 1-27. The Examiner previously withdrew claims 11-24 and 27 from consideration. Consequently, claims 1-10, 25, and 26 are pending. In the outstanding Office Action, the Examiner (1) made a Response to Arguments, (2) rejected claims 1, 7-10, 25, and 26 under 35 USC §102(e), (3) rejected claims 2 and 3 under 35 USC §103(a), and (4) objected to claims 4-6 as being dependent on a rejected base claim but indicated these claims would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Rejection of Claims 1, 7-10, 25, and 26 Under 35 USC §102(e)

The Examiner rejected claims 1, 7-10, 25, and 26 as being anticipated under 35 USC §102(e) by Carl Stevenson, U.S. Patent No. 6,209,112 (hereinafter, "Stevenson"). In particular, the Examiner asserts that Stevenson teaches reducing power consumption in a decoder of the error correction system when the actual number of errors is less than the maximum error correction capability.

Applicant respectfully traverses this rejection. Stevenson discloses that:

> "a datablock is received comprising a first checksum value and an encoded payload, the encoded payload having at least one parity value and the data. A second checksum value is calculated for the encoded payload, and then the first checksum value and the second checksum value are compared. *If the first checksum value is equivalent to the second checksum value, then the at least one parity bit value is removed and the encoded payload is provided as the error-corrected data. If, however, the first checksum value is not equivalent to the second checksum value, then error-correction processing of the encoded payload is enabled based on the at least one parity bit value to provide the error-corrected data.*"
> (Col. 2, lines 35-46; emphasis added.)

Stevenson also discloses "[e]nabling error-correction only when required conserves power of, for example, a battery of the wireless unit." (Stevenson at col. 2, lines 32-34.) Thus, Stevenson does ***not*** teach to performing error correction in a *reduced power mode.* Independent claims 1, 25, and 26, as amended, require performing error correction in a reduced power mode in a decoder of the error correction system when the actual number of errors is less than the maximum error correction capability.

As an example of these limitations, Applicant states the following at page 14, line 27 to page 15, line 4:

> Second, when the number of errors that actually occur is smaller than t, i.e., the maximum number of symbol errors that an RS(n, n - $2t$) code can correct, the Euclidean algorithm converges within less than $2t$ iterations. A small control circuit 990 is used to detect early convergence of the algorithm (i.e., when either $\deg(R(x)) < t$ or $\deg(Q(x)) < t$ is satisfied), download the resulting polynomials, and put the entire block into low power "Opcode = 0" mode 945. Under normal operating conditions, the actual number of errors in each block is usually much smaller than t. Consequently, the additional "Opcode = 0" mode 945 leads to great power savings.

The cited text describes an example of how, when an actual number of errors is less than a maximum error *correction* capability of a Reed-Solomon error correcting code, a block in a decoder can be placed in *low power mode*.

Therefore, Stevenson does not disclose or suggest performing error correction in a reduced power mode in a decoder of the error correction system when the actual number of errors is less than the maximum error correction capability, and as set forth in independent claims 1, 25, and 26, as amended.

Also, as argued in the previous Response to Office Action, it is important to note that Applicant's independent claims require a known maximum error *correction* capability (e.g., t in the cited text above). While Stevenson does disclose that error correction can be performed, a maximum error correction capability is *not* used to determine whether error correction is or is not performed in Stevenson. Although the Examiner asserts that error correction decoders for Reed-Solomon, Hamming or Golay codes first determine the number of errors in a codeword and then determine if the codeword is detectable, Applicant could find ***no*** such disclosure in Stevenson. In fact, Stevenson teaches that:

> Next at ***506*** the *error-correction is performed for the datablock* and then at step 508 the data of the encoded payload is provided to the user. In an alternative embodiment, *if the error-correction process of step **506** determines that an error cannot be corrected, then the data is corrected to the best of the ability of the error-correction processor* and then flagged as bad data at step 507.
> Col. 7, lines15-21.

A person of ordinary skill in the art would ***not*** read Stevenson to suggest the step of determining if an actual number of errors is less than a maximum error correction capability.

Therefore, Stevenson does ***not*** disclose or suggest that a determination is made as to whether an actual number of errors is less than a maximum error correction capability, and as set forth in independent claims 1, 25, and 26, as amended.

Consequently, Applicant respectfully submits that independent claims 1, 25, and 26 are patentable over Stevenson and requests the §102(e) rejection to these claims be withdrawn. Because independent claim 1 is patentable, its dependent claims 7-10 are also patentable for at least the reasons given above.

Rejection of Claims 2 and 3 Under 35 USC §103(a)

Because independent claim 1 is patentable over the cited art, claims 2 and 3, which include all limitations of independent claim 1, are also patentable.

Conclusion

Applicant respectfully submits that claims 1-3, 7-10, 25, and 26 are patentable over the cited art, alone or in combination. The Examiner's attention to this matter is appreciated.

Respectfully submitted,

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